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MAIL STOP AMENDMENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: T. Hironaka et al. Attorney Docket No.: SUSU121842

Application No.: 10/687,460 Art Unit: 2188 / Confirmation No.: 8870

Filed: October 15, 2003

Title: MULTI-PORT INTEGRATED CACHE

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Seattle, Washington 98101

February 3, 2006

TO THE COMMISSIONER FOR PATENTS:

Applicants are aware of the information listed in the attached form that may be material to the prosecution of the above-identified patent application.

1. __X__ Copies of the listed publications and non-patent literature are enclosed for the Examiner's use.

2. __X__ A concise explanation of the relevance of document Cite Nos. F1-F2 (which are not in the English language), as presently understood by the individual designated under 37 C.F.R. § 1.56(c) most knowledgeable about their content, is provided. The statement of relevancy for each reference is stated below.

F1. Describes the cache memory device having m-number bus terminals BA adds the cache memory CSB which is provided with k(k<m)-number cache memory ports for reading data from the cache memory CSB and p(p<m)-number cache memory ports for writing data to the cache memory, a connection area KF providing a connection between the cache memory ports and the bus terminals BAs and a cache memory control part CCU for controlling connection elements BK of the connection area KF.

F2. Describes the conventional multi-port cache memory is excellent in high speed since it is constituted by using multi-port cell blocks, however, chip size is increased when erroneous cache is attempted to be reduced by increasing its capacity since the areas of the cell blocks to be components increase in proportion to square of the number of ports, which becomes a cause of cost increase. The large capacity multi-port cache memory having random access band width, to which parallel access from plural ports are enabled and suitable for use for the most advanced microprocessor with low probability of the erroneous cache is easily provided since the multi-port cache memory is formed by using one port cell block suitable for capacity increase as the component.

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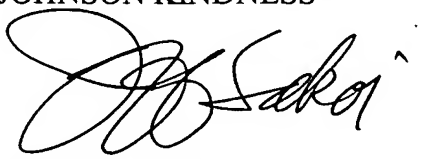
3. __X__ Pursuant to 37 C.F.R. § 1.97(b), this Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits.

4. __X__ The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to Deposit Account No. 03-1740.

Respectfully submitted,

CHRISTENSEN O'CONNOR
JOHNSON KINDNESS PLLC



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I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid and addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date.

Date: 2/3/06 Shannon Lih

JMS:snh

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INFORMATION CITED BY APPLICANTS THAT MAY BE MATERIAL TO THE PROSECUTION OF THE SUBJECT APPLICATION

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U.S. PATENT DOCUMENTS

*Examiner Initials	Cite No.	Document No.	Kind Code	Date (mm/dd/yyyy)	Name
None					

FOREIGN PATENT DOCUMENTS

*Examiner Initial	Cite No.	Document No.	Kind Code	Publication Date (mm/dd/yyyy)	Country	English Abstract Provided	English Translation Provided
_____	F1	JP 4-257949	A	09/14/1992	JP		
_____	F2	JP 2002-55879	A	02/20/2002	JP		

OTHER INFORMATION
(Including Author, Title, Date, Pertinent Pages, Etc.)

*Examiner Initial	Cite No.	
_____	O5	Mattausch, H.J., "Hierarchical N-Port Memory Architecture Based on 1-Port Memory Cells," Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima, Japan, p. 348-352.

Examiner **Date Considered**

_____ _____

*Examiner: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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